A New Approach to DRC: the Calibre nm Platform

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Through many years of semiconductor process evolution, the impact of manufacturing limitations and variations on layout could be encapsulated in relatively simple design rules. Design rule checking enforced these manufacturing constraints by comparing a characteristic measurement to a threshold value. Layout patterns either passed or failed these checks, with failures being fixed to ensure a DRC-clean sign-off.

Then along came nanometer process technology, where increasing rates of silicon failure and longer yield ramps initiated a sea change in how designers deal with process constraints. Designers now find they can no longer adequately describe the effects of process limitations and variations using design rules alone. Most urgently, compliance with design rules no longer always guarantees acceptable yields.

Here is why: Simple design rule checks alone no longer account for the variety and complexity of situations that occur in nanometer processes. For example, unexpected catastrophic layout failures arise from layout 'shorts' and 'opens' due to random defects believed accounted for and from lithography limitations that cause bridging and pinching.

To ensure high yields when using nanometer process technology, designers require new information and new levels of judgment that go beyond design rule checking to yield analysis. They need new ways to assess the quality of their designs in light of the more complex process constraints and larger process variations they now face. They need new ways to see the impact these constraints and variations have on the quality of their designs. Finally, they need a new kind of work environment that allows them to understand which of these effects is the most important to address during the process of improving design quality.

From Pass/No Pass to Statistical Yield Analysis

Advanced design rule checking now incorporates statistical yield modeling, rather than just threshold comparison. Layout database characteristics can now be extracted and represented as statistical distributions. Designers gain insight into the range of results in comparison to both compliance thresholds and recommended rule values. Yield models applied to these results prioritize them by providing the designer with a design quality score. New visualization tools allow a designer to select the highest priority result and work on it in his preferred layout environment.

Designers can also now apply two advanced analytical techniques, critical area analysis and litho-friendly design checking, during sign-off to improve design quality and design robustness.

Critical area analysis enables the designer to understand a layout's sensitivity to a range of defect sizes. It also provides an estimate of cumulative particle yield impact by combining layout sensitivity with actual particle size distributions expected during manufacture.

Litho-friendly design checking transforms the complexities of the lithography process into simple DRC-like results that guide designers to weak points in the layout. These weak points represent portions of the layout at risk of bridging or pinching due to variations in the lithography process.

Designers will soon be able to combine the results of all four of these techniques, design rule checking, statistical yield modeling, critical area analysis and litho-friendly design checking, to arrive at a comprehensive picture of design quality. While the risks associated with manufacturing sign-off have increased markedly with the onset of nanometer process technology, design rule checking has evolved to yield analysis, enabling designers to meet these new challenges and achieve high quality, production-worthy designs.

Improving Run and Cycle Times in Nanometer Designs

An important issue surrounding the ability to perform a comprehensive nanometer sign-off is the capability to manage run times. The actual runtime during a DRC cycle has always been a target for reducing cycle time. Reducing runtime can be done in several ways such as using faster hardware, optimizing DRC commands to improve efficiency, optimizing the engine for faster data processing, and better distributing operations on the available hardware.

Scaling is a metric that is often used to give some indication as to how well the application is utilizing the hardware it was submitted on. For example, perfect scaling on 10 CPUs would be a scaling index of 10; however, linear scaling is not likely. That would require all 10 CPUs to be utilized throughout the entire job and no overhead to manage the process. But there are inherent problems in using scaling alone as the yardstick by which to measure DRC tool performance. While scaling *is* important, it's not the whole story.

The time a designer spends debugging a design is arguably the longest in the DRC cycle. A robust debug environment and overall cycle time are often overlooked when DRC tools are evaluated. However, a robust debug environment provides designers with the capability to quickly identify, fix, and re-verify their design and may have the biggest impact in overall cycle time to tape-out.

How is cycle time being reinvented?

First, new architecture improvements in the DRC processing engine partitions design data so that operations can be paralleled on multiple CPUs. This way, all CPUs on the network are equally utilized, with none sitting idle. By making more efficient and intelligent of use of available CPUs, the result is much faster overall physical verification run time, setting the stage for faster cycle time.

Second, incremental verification enables designers to begin debugging soon after the DRC run begins, instead of waiting until the run is complete. This allows a parallel debugging process. Incremental capabilities also give designers the option to check only part or parts of a design, or a subset of the required sign-off rules. Designers may prefer to perform incremental verification between DRC cycles that check the entire design to ensure modifications made were done so correctly.

Translation time, too, can rob a project schedule of precious hours. Eliminating it can enable a verification engineer to complete more cycles in a given day or spend more time debugging results.

While some forms of incremental have been previously available—area based DRC and select check DRC—parallel debugging promises to re-invent the current debug process. It continually generates DRC results, loading them into a results viewing environment as operations complete in parallel with the DRC run time. This improves productivity many times over as designers can fix errors in real time, shortening iteration times, and improving time to sign-off.

Conclusion

Nanometer processes have not only redefined the expectations of a DRC-clean sign-off but also the way in which designers perform a sign-off. Comprehensive analysis checks and faster cycle times are necessary in order to manage design in the nanometer era. Employing a re-architected DRC processing engine that enables designers to step into the nanometer era is the key to success.

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